**June 18th Senior Project Meeting**

**Armstrong 144, 3:30 P.M – 5:05 P.M.**

**Members in Attendance:** Dr. Pearlstein, Zachary Nelson, Julie Swift, Whitley Forman and Dhruvit Naik

* Went through the CORE requirements hierarchy for the chip **(System Design Step)**
  + Zach will make the top-level requirements the elements from the chip block diagram so that the requirements are broken down in a more logical way
  + Zach will make an Enhanced Functional Flow Block Diagram (EFFBD) on CORE with the functions that were generated as part of creating the requirements
* Discussed the design flow of creating an integrated circuit
  + A figure illustrating this is on GitHub under Chip-Design/proj\_asic/docs/design\_flow.png
  + Major Steps
    - System Design
    - RTL Design
    - Logic Synthesis
    - Design for Test (DFT) Implementation – may be able to skip this
    - Floor Planning
    - Place and Optimization
    - Routing
    - Verification
* Deadline for the chip
  + November 30th: We would get the chip back in the Spring semester and be able to see if it works
  + March 2016: Would get the chip back after graduation and would implement our design on a FPGA during the Spring semester instead
* Dropbox will be used for storing private files
  + The rest of the code and documents will be stored on the public GitHub account
* Assigned Verilog modules to group members **(RTL Design Step)**
  + Everyone will start working on the modules over the summer
  + Zach: i2s\_in.v and i2s\_out.v
  + Julie: register.v
  + Whitley: i2c\_slave.v
  + Dhruvit: filter.v
  + Kevin: chip.v
* Julie and Whitley need to hand in the NDA forms (electronically or in person)
* Kevin and Dhruvit need to accept the invite to the GitHub account